

List of Safety Requirements

Nº	ID	Name	Description	Kind	ASIL	Time constraint	Physical constraint	Comment	Traced FTA Events	Status	Related Goals	Coordinatoribus	Coordinatoribus To	Allocations
1	SR020	Insulation resistance measurement performance	The BMS shall measure insulation resistance with range at least of xxx to xxx Mohm with accuracy of +- xxx Mohm at most and resolution of xxx Mohm at most and a sampling rate of at least xxx sample/sec	TECHNICAL	A				no traced events	PROPOSED	• SR341 (ASIL D) • SR343 (ASIL D)	• SR013 (ASIL A) • SR011 (ASIL B) • SR007 (ASIL B)	• SR01 (ASIL A)	Insulation Monitoring • BJB IC • MCU • TPL Transciever
2	SR022	HV switch timing	The BMS shall be able to open and close the HV switches of the battery	TECHNICAL	B				no traced events	PROPOSED	• SR243 (ASIL B) • SR011 (ASIL B) • SR007 (ASIL B)	• SR015 (ASIL B) • SR01 (ASIL B) • SR007 (ASIL B)	• FET / Contactor Driver (ASIL B) • MCU	

2.1	SR02 3	Current Integrator HV switch timing	The BMS shall be able to open and close the HV switches of the battery upon a Current Integrator signal assignment within xxx ms and xxx ms respectively, preferably implemented in HW	TE CH NIC AL	B				no traced events	PR OP OS ED				• FET / Contactor Driver (ASIL B) • Short-circuit detection • FET / Contactor
3	SR02 4	Gas and/or pressure measurement performance	The BMS shall measure xxx gas(es) with at least range of xxx to xxx PPM with accuracy of +- xxx PPM at most and resolution xxx PPM at most and/or pressure with at least range of xxx to xxx bar at most with accuracy of xxx bar and resolution of xxx bar at most and a sampling rate of at least xxx sample/sec	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 34 6 (AS IL D)	• SR 02 7 (AS IL B)	• MCU	• SR 34 7 (AS IL D)

4	SR025	Battery temperature measurement performance	The BMS shall measure battery temperature with at least range of xxx to xxx C° with accuracy of +- xxx C° at most and resolution xxx C° at most and a sampling rate of at least xxx sample/sec	TE CH NIC AL	B					no traced events	PR OP OS ED	• SR 35 3 (AS IL D) • SR 35 4 (AS IL D)	• SR 00 8 (AS IL B) • SR 00 5 (AS IL B)	• MCU • AFE • TPL Transciever
5	SR027	TR detection algorithm	The BMS shall include an algorithm to predict TR event based on temperature and gases and/or pressure within xxx sec from it's occurrence	TE CH NIC AL	B					no traced events	PR OP OS ED	• SR 02 4 (AS IL B) • SR 36 2 (AS IL D) • SR 36 3 (AS IL D) • SR 36 4 (AS IL D)	• SR 00 5 (AS IL B) • SR 36 2 (AS IL D) • SR 36 3 (AS IL D) • SR 36 4 (AS IL D)	• MCU

6	SR034	Cell voltages monitor performance	The BMS shall measure cell voltages with range at least of xxx to xxx V with accuracy of +/-xxx mV at most and resolution of xxx mV at most and a sampling rate of at least xxx sample/sec	TE CH NIC AL	B					no traced events	PR OP OS ED	• SR 36 5 (AS IL C(D)) • SR 36 6 (AS IL D)	• SR 00 6 (AS IL B)	• MCU • AFE • TPL Transciever
7	SR036	Battery current monitor performance	The BMS shall measure battery current with range at least of xxx to xxx A with accuracy of +/-xxx A at most and resolution of xxx A at most and a sampling rate of at least xxx sample/sec	TE CH NIC AL	B					no traced events	PR OP OS ED	• SR 38 1 (AS IL D) • SR 38 2 (AS IL D) • SR 03 0 (AS IL B)	• SR 01 2 (AS IL B)	• MCU • BJB IC • TPL Transciever

8	SR03 9	Dynamic Current Limit message	The BMS shall compose and transmit a periodical message containing the maximum recommended discharging current, and charging current, as calculated by the Dynamic Current Limit	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 39 4 (AS IL D)	• SR 00 9 (AS IL B)	• MCU • CAN Transciever
9	SR04 0	DCL_STATUS: OVERLOAD	The BMS shall set the Flag DCL_STATUS to OVERLOAD in case the Dynamic Current Limit algorithm detects further increase in temperature due to overload	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 00 9 (AS IL B)	• MCU	

10	SR04 1	DCL_ST ATUS: NORMAL	The BMS shall set the Flag DCL_STATU S to NORMAL if the Dynamic Current Limit algorithm does not detect an overload during a time period as specified in the configuratio n parameter DCL_OVERL OAD_TIME OUT	TE CH NIC AL	B					no traced events	PR OP OS ED			• SR 00 9 (AS IL B)	• MCU
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11	SR042	Set flags when system is outside of, or about to breach temperature SOA condition		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 48 00 2 2 (AS (AS IL IL D) B) • SR 48 01 6 0 (AS (AS IL IL D) B) • SR 49 9 (AS IL D) • SR 14 3 (AS IL B) • SR 49 1 (AS IL D) • SR 49 5 (AS IL D) • SR 50 3 (AS IL D) • SR 50 7 (AS IL D) •	• SR 48 00 2 2 (AS (AS IL IL D) B) • SR 48 01 6 0 (AS (AS IL IL D) B) • SR 49 9 (AS IL D) • SR 14 3 (AS IL B) • SR 49 1 (AS IL D) • SR 49 5 (AS IL D) • SR 50 3 (AS IL D) • SR 50 7 (AS IL D) •	• MCU
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											SR 50 5 (AS IL D)		
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12	SR04 3	Set flags when system in is outside of, or about to breach cell voltage SOA condition	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 14 8 • SR 51 2 • SR 51 6 • SR 51 9 • SR 52 2 • SR 52 7 • SR 52 5 • SR 52 9 •	• SR 00 3 (AS IL B) • SR 01 0 (AS IL D) • (AS IL D) • (AS IL D) • (AS IL D) • (AS IL D) • (AS IL D) • (AS IL D) • (AS IL D)	• MCU
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											SR 53 1 (AS IL D)		
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13	SR04 4	Set flags when system in is outside of, or about to breach current SOA condition	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 14 9 (AS IL B) • SR 15 0 (AS IL B) • SR 15 1 (AS IL B) • SR 15 2 (AS IL B) • SR 15 3 (AS IL B) • SR 15 4 (AS IL B) • SR 15 5 (AS IL B) • SR 15 6 (AS IL B)	• SR 00 4 (AS IL B) • SR 01 0 (AS IL B) • SR 15 1 (AS IL B) • SR 15 2 (AS IL B) • SR 15 3 (AS IL B) • SR 15 4 (AS IL B) • SR 15 5 (AS IL B) • SR 15 6 (AS IL B)	• MCU
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14	SR045	Set flags when battery is out of balance		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 05 3 (AS IL B) • SR 05 4 (AS IL B) • SR 05 5 (AS IL B) • SR 05 6 (AS IL B)	• SR 01 0 (AS IL B) • MCU
15	SR046	Start balancing battery	The BMS shall balance the cells while the Flag CELL_BALANCE_STATUS is in state UNBALANCE	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 01 6 (AS IL B)	• MCU • AFE • TPL Transciever

16	SR04 7	Battery voltages monitor performance	The BMS shall measure battery voltage with range at least of 0 to xxxV with accuracy of xxx mV at most and resolution of xxxmV at most and a sampling rate of at least xxx sample/sec	TE CH NIC AL	B					no traced events	PR OP OS ED	• SR 39 8 (AS IL D)	• SR 01 8 (AS IL B)	• MCU • BJB IC • TPL Transciever
16.	SR04 1 8	Battery voltages monitor range	The BMS shall measure battery voltage with range at least of 0 to xxxV	UN SP ECI FIE D	B					no traced events	PR OP OS ED			
16.	SR04 2 9	Battery voltages monitor accuracy		UN SP ECI FIE D	D					no traced events	PR OP OS ED			

17	SR050	Set flags when system in is outside of, or about to breach battery voltage SOA condition		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 07 7 (AS IL B) • SR 07 8 (AS IL B) • SR 07 9 (AS IL B) • SR 08 0 (AS IL B) • SR 08 1 (AS IL B)	• SR 01 0 (AS IL B) • MCU
18	SR057	Protect against faulty measurement spikes by filtering		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 40 8 (AS IL D) • SR 40 9 (AS IL D)	• SR 01 7 (AS IL B) • MCU

18.1	SR058	Filter measurement	The BMS shall include filters for all measurements to filter out data spikes xxx	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
18.1.1	SR059	Detect out-of-range battery voltage measurements		TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
18.1.2	SR060	Detect out-of-range current measurements		TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
18.1.3	SR061	Detect out-of-range temperature measurements		TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
18.1.4	SR063	Detect out-of-range cell voltage measurements		TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU

19	SR06 4	Temporary disconnect the battery if overtemperature has been detected in BMS		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 40 1 (AS IL D) • SR 41 0 (AS IL D) • SR 41 1 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
19. 1	SR06 5	Close switches at IC_TEMP_STATUS: NORMAL	The BMS shall assign signal(s) as to close the HV switches of the battery and charger upon Flag IC_TEMP_STATUS set to NORMAL if no other protections are activated that require open HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor

19.	SR07 2	Open switches at IC_TEMP_STATUS: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag IC_TEMP_STATUS set to any of the following: - OVERTEMPERATURE_AF - OVERTEMPERATURE_BJ - OVERTEMPERATURE_MCU - OVERTEMPERATURE_SB - OVERTEMPERATURE_SHUNT - OVERTEMPERATURE_HV_SWITCH	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
20	SR07 5	Notify driver and passengers about fault and warning condition of the HV Switch		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 41 5 (AS IL D)	• SR 02 9 (AS IL B)	• MCU	

20.1	SR076	HV_SWITCH_STATUS: FAILURE	The BMS shall set the Flag HV_SWITC H_STATUS to FAILURE upon a detection of the event via the HV Switch failure detection algorithm. The parameters of this algorithm shall be stored in the configuration file	TE CH NIC AL	B					no traced events	PR OP OS ED					• MCU
20.2	SR082	HV_SWITCH_STATUS: NORMAL	The BMS shall set the Flag TR_STATUS to NORMAL upon clearing of the event via the HV Switch failure detection algorithm	TE CH NIC AL	B					no traced events	PR OP OS ED					• MCU

21	SR083	Protect BMS from undesired effects of uncontrolled uC power-down		TECHNICAL	B				no traced events	PROPOSED	• SR419	• SR017	• MCU (ASIL B)	• SBC
21.	SR0814	Brownout		TECHNICAL	B				no traced events	PROPOSED			• MCU	• SBC (ASIL B)

22	SR085	Notify the driver and passengers about BMS overtemperature	TECHNICAL	B				no traced events	PROPOSED	• SR072 (AS ILB)	• SR029 (AS ILB)	• SR071 (AS ILB)	• SR070 (AS ILB)	• SR069 (AS ILB)	• SR068 (AS ILB)	• SR067 (AS ILB)	• SR066 (AS ILB)
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23	SR086	Permanently disconnect the battery if Mosfets/Contactor is faulty		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR416 (ASIL D)	• SR028 (ASIL B)	• MCU • FET / Contactor Driver • FET / Contactor
23.1	SR654	SM: Recover y out of permanent failure shall only be possible through service station intervention.		TE CH NIC AL	B				no traced events	PR OP OS ED			
24	SR087	Continuously monitor BMS internal temperatures		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR026 (ASIL B)	• MCU • AFE • SBC (ASIL B) • BJB IC • TPL Transciever • Onboard thermistor[0..*]	
24.1	SR088	IC die temperature measurements	The AFE, BJB, MCU, SBC main ICs of the BMS shall include internal temperature measurements to assess and prevent possible failures associated	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU • SBC (ASIL B) • BJB IC • AFE • TPL Transciever	

24.	SR08	Make BMS enter fault state in case of either of MCU, AFE, or SBC reaching high die temperature		TE CH NIC AL	B				no traced events	PR OP OS ED			
24.	SR09	Recover BMS from fault state to normal state when temperatures are within permissible operating range for each part on the BMS		TE CH NIC AL	B				no traced events	PR OP OS ED			
24.	SR09	Shunt temperature measurement performance	The BMS shall measure Shunt temperature with at least range of xxx to xxx C° with accuracy of +- xxx C° at most and resolution xxx C° at most and a sampling rate of at least xxx sample/sec	TE CH NIC AL	B				no traced events	PR OP OS ED			<ul style="list-style-type: none"> • MCU • Onboard thermistor[0..*] • TPL Transciever • BJB IC

24.	SR093	HV Switch temperature measurement performance	The BMS shall measure HV Switch temperature with at least range of xxx to xxx C° with accuracy of +- xxx C° at most and resolution xxx C° at most and a sampling rate of at least xxx sample/sec	TE CH NIC AL	B					no traced events	PR OP OS ED					• MCU • Onboard thermometer[0..*] • TPL Transciever • BJB IC	
25	SR093	Perform BIST		TE CH NIC AL	B					no traced events	PR OP OS ED	• SR 12 8 (AS IL B)	• SR 02 6 (AS IL B)	• SR 13 4 (AS IL B)	• SR 42 2 (AS IL D)	• SR 42 3 (AS IL D)	• MCU • SBC (ASIL B) • AFE • BJB IC • TPL Transciever

25.	SR09 4	IC self test	The AFE, BJB, MCU, SBC main ICs of the BMS shall include internal Build In Self Test (BIST) to assess and prevent possible random and latent failures	TE CH NIC AL	B				no traced events	PR OP OS ED				• AFE • MCU • SBC (ASIL B) • BJB IC • TPL Transciever
26.	SR09 5	Continuously monitor HV FETs voltages		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 42 5 (AS IL D) • SR 43 2 (AS IL D)	• SR 02 6 (AS IL B)	• SR 02 6 (AS IL B)	• Insulation Monitoring • MCU • TPL Transciever • BJB IC
26.	SR09 6	HV voltage measurement performance	The BMS shall measure both HV Switch voltages (HV input and output) with range at least of -xxx to xxxV with accuracy of xxx mV at most and resolution of xxxmV at most and a sampling rate of at least xxx sample/sec	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • Insulation Monitoring • TPL Transciever • BJB IC

26.	SR09 2	HV Switch failure detectio n algorith m	The BMS shall include an algorithm to detect failure of the HV Switch based on the input and output voltage measureme nts within xxx sec from it's occurrence	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
26.	SR09 2.1	Detect HV switch failure in short 8		TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
26.	SR09 2.2	Detect HV switch failure in open 9		TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
27	SR10 0	Tempora ry disconne ct the battery if external commun ication errors have been detected in BMS		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 43 4 IL • SR 43 5 (AS IL D)	• SR 02 8 (AS IL B)	• ASIL B • FET / Driver • FET / Contactor	• FET / Contactor

27.1	SR10	Close switches at EXT_CO M_STAT US: NORMAL	The BMS shall assign signal(s) as to close the HV switches of the charger and the battery upon a EXT_COM_STATUS to NORMAL within xxx ms	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
27.2	SR10	Close switches at EXT_CO M_STAT US: WARNING or NORMAL	The BMS shall assign signal(s) as to close the HV switches of the battery and charger upon Flag EXT_COM_STATUS set to any of the following: - EXT_COM_WARN - NORMAL if no other protections are activated that require open HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor

27.3	SR105	Open switches at EXT_CO M_STAT US: TIMEOUT T	The BMS shall assign signal(s) as to open the HV switches of the battery upon a EXT_COM_STATUS to TIMEOUT within xxx ms	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
27.4	SR106	Open switches at EXT_CO M_STAT US: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag EXT_COM_STATUS set to EXT_COM_FAILURE	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
28	SR107	Protect BMS from hanging		TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 017 (ASIL B)	• MCU • SBC (ASIL B)	
28.1	SR108	Watchdog	The BMS shall be reset in case the Watchdog(s) did not receive periodic pulses as specified in configuration parameter(s)	TE CH NIC AL	B				no traced events	PR OP OS ED			• MCU • SBC (ASIL B)	

29	SR109	Temporary disconnect the battery if bit-flip has been detected in memory		TE CH NIC AL	B				no traced events	PR OP OS ED		• SR028 (ASIL B) ILB)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
29.1	SR110	Close switches at MEMORY_STATUSES: WARN or NORMAL	The BMS shall assign signal(s) as to close the HV switches of the battery and charger upon Flag COM_STATUS set to any of the following: - MEMORY_ECC_WARN - NORMAL if no other protections are activated that require open HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor	
29.2	SR111	Open switches at MEMORY_STATUSES: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag MEMORY_STATUS set to MEMORY_ECC_FAILURE	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor	

30	SR11 2	Notify the driver and passengers about BMS external communication error		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 43 6 (AS IL D)	• SR 02 9 (AS IL B)	• SR 12 1 (AS IL B)	• MCU
30.	SR11 1 3	- EXT_CO M_FAILU RE_TIME OUT - COMS_S TATUS: TIMEOU T	The BMS shall assign the Flag EXT_COM_STATUS to TIMEOUT upon failure to receive regular communication from external controller for a period equal to or greater than specified in configuration parameter EXT_COM_FAILURE_TIMEOUT presented in ms	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU

30.2	SR114	EXT_COMM_STATUS: NORMAL	The BMS shall set the Flag EXT_COM_STATUS to NORMAL upon no CRC error nor EDC being necessary in external communication	TECHNICAL	B				no traced events	PROPOSED					• MCU
30.3	SR115	EXT_COMM_STATUS: EXT_COMM_WARN	The BMS shall set the Flag EXT_COM_STATUS to EXT_COM_WARN upon detected CRC error and successful correction of the error by the EDC in external communication	TECHNICAL	B				no traced events	PROPOSED					• MCU
30.4	SR116	EXT_COMM_STATUS: EXT_COMM_FAILURE	The BMS shall set the Flag EXT_COM_STATUS to EXT_COM_FAILURE upon detected CRC error and inability of the EDC to correct the error in external communication	TECHNICAL	B				no traced events	PROPOSED					• MCU

31	SR117	Notify driver and passengers about internal memory errors	Memory bit-flip	TECHNICAL	B				no traced events	PROPOSED			• SR029 (ASIL B)	• MCU
31.1	SR118	MEMORY_STATUSES: MEMORY_ECC_FAILURE	The BMS shall set the Flag MEMORY_STATUS to MEMORY_ECC_FAILURE upon detected of any memory error by the ECC and inability to correct it	TECHNICAL	B				no traced events	PROPOSED				• MCU
31.2	SR119	MEMORY_STATUSES: MEMORY_ECC_WARN	The BMS shall set the Flag MEMORY_STATUS to MEMORY_ECC_WARN upon detected of any memory error by the ECC and successful correction of it	TECHNICAL	B				no traced events	PROPOSED				• MCU
31.3	SR120	MEMORY_STATUSES: NORMAL	The BMS shall set the Flag MEMORY_STATUS to NORMAL upon no memory error being detected by the ECC of any memory	TECHNICAL	B				no traced events	PROPOSED				• MCU

32	SR12 1	Continuously monitor BMS external communications		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 11 2 (AS IL B) • SR 10 0 (AS IL B) • SR 43 7 (AS IL D) • SR 43 9 (AS IL D) • SR 44 0 (AS IL D)	• SR 02 6 (AS IL B) • MCU
32.	SR12 1 2	EDC on external communication	The external BMC communication shall include EDC to correct possible communication errors	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU

32.2	SR124	CRC on external communication	The external BMS communication shall include CRC to detect possible communication errors	TECHNICAL	B				no traced events	PROPOSED					• MCU
32.3	SR125	Periodic external communication timers	The BMS shall keep timers associated to periodic communication packets with external controller and reset them for every packet that was successful received	TECHNICAL	B				no traced events	PROPOSED					• MCU
33	SR126	Implement ECC in all memories		TECHNICAL	B				no traced events	PROPOSED		• SR026 (ASILB)	•	MCU	
33.1	SR127	ECC memory	All memory of used in the BMS shall include ECC	TECHNICAL	B				no traced events	PROPOSED				• MCU	
34	SR128	Notify driver and passengers about BIST detected failure		TECHNICAL	B				no traced events	PROPOSED		• SR029 (ASILB)	• SR093 (ASILB)	• MCU	

34.1	SR129	IC_BIST_STATUS: BIST_FA ILURE_SBC	The BMS shall set the Flag IC_BIST_STATUS to BIST_FAILURE_SBC upon inability of the SBC's BIST to complete successfully	TECHNICAL	B				no traced events	PROPOSED					• MCU
34.2	SR130	IC_BIST_STATUS: BIST_FA ILURE MCU	The BMS shall set the Flag IC_BIST_STATUS to BIST_FAILURE MCU upon inability of the MCU's BIST to complete successfully	TECHNICAL	B				no traced events	PROPOSED					• MCU
34.3	SR131	IC_BIST_STATUS: BIST_FA ILURE_BJB	The BMS shall set the Flag IC_BIST_STATUS to BIST_FAILURE_BJB upon inability of the BJB's BIST to complete successfully	TECHNICAL	B				no traced events	PROPOSED					• MCU

34.	SR13 4	IC_BIST_Status: BIST_FA ILURE_A FE	The BMS shall set the Flag IC_BIST_STATUS to BIST_FAILURE_AFE upon inability of the AFE's BIST to complete successfully //vtpl-dngsrvapp: 50000/ RM:user=d b2amin;password={password};	FU NC TIO NA L	B					no traced events	PR OP OS ED				• MCU
34.	SR13 5	IC_BIST_Status: NORMAL	The BMS shall set the Flag IC_TEMP_STATUS to NORMAL upon completion of all BIST completed successfully	TE CH NIC AL	B					no traced events	PR OP OS ED				• MCU
35	SR13 4	Temporary disconnect the battery if BIST detected failure in BMS		TE CH NIC AL	B					no traced events	PR OP OS ED				• MCU • FET / Contactor SR 028 (ASIL B) • FET / Contactor SR 093 (ASIL B)

35.1	SR157	Close switches at IC_BIST_STATUSES: NORMAL	The BMS shall assign signal(s) as to close the HV switches of the battery and charger upon Flag IC_BIST_STATUS set to NORMAL if no other protections are activated that require open HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
35.2	SR160	Open switches at IC_BIST_STATUSES: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag IC_BIST_STATUS set to any of the following: - BIST_FAILURE_AFE - BIST_FAILURE_BJB - BIST_FAILURE MCU - BIST_FAILURE_SBC	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
36	SR161	Provide BMS with absolute time		TE CH NIC AL	B				no traced events	PR OP OS ED			• SR 01 7 (AS IL B)	• MCU

36.1	SR162	Absolute time life	The BMS shall include an absolute timer that is self powered with sufficient energy to count time for up to xxx days from when the BMS was last powered	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
36.2	SR163	Absolute time resolution	The BMS shall track absolute time with a resolution of seconds and an accuracy of xxx PPM	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
37	SR164	Provide BMS counter for timestamped Reset events		TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 01 7 (AS IL B)	• MCU	
37.1	SR165	Store RESET Count in NV memory	The BMS shall include sufficient NV memory to store the absolute time of the last boot and the RESET_COUNT Flag for at least 100 entries	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU

37.2	SR166	Access RESET Count	The BMS shall allow access of the RESET Count file in memory download mode	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
38	SR167	Maintain proper operation at re-boot		TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 017 (AS IL B)	• CAN Transciever	
38.1	SR168	Store configuration & Flags	The BMS shall include sufficient NV memory to store the configuration file and Flags	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
38.2	SR169	Retrieve configuration & Flags at boot	At boot the BMS will retrieve the configuration and Flags from NV memory	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
38.3	SR170	Program configuration & Flags	Configuration file and Flags in NV memory shall be able to be programmed by the BMS in configuration upload and Flag clearance mode respectively	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • CAN Transciever

39	SR17 1	HV or leakage FAULT counter and FAILURE assignm ent	Keep a FAULT counter for the amount the insulation resistance measurement has been detected to be lower than a threshold. When the counter registers a certain amount assign a FAILURE.	TE CH NIC AL	A				no traced events	PR OP OS ED		• SR 00 1 (AS IL A)	• MCU
39.	SR17 1 2	HV_STATUS: FAULT	The BMS shall set the Flag HV_STATUS to FAULT upon a valid measurement of insulation resistance lower than specified in configuration parameter INS_RES_THR	TE CH NIC AL	A				no traced events	PR OP OS ED		• SR 44 3 (AS IL D)	• MCU

39.2	SR173	HV_STATUSTUS: NORMAL	The BMS shall set the Flag HV_STATUS to NORMAL upon a valid measurement of insulation resistance higher or equal than specified in configuration parameter INS_RESTHR	TECHNICAL	A				no traced events	PROPOSED	• SR442 (ASILD)	• MCU
39.3	SR174	HV_FAULT_COUNTHV_STATUSTUS: FAILURE	The BMS shall keep a counter HV_FAULT_COUNT in Flag HV_STATUS of the times the Flag is assigned to FAULT and cleared again. Upon counting an amount equal to or higher than specified in configuration parameter HV_FAULT_COUNT_LIMIT the Flag HV_STATUS shall be set to FAILURE.	TECHNICAL	A				no traced events	PROPOSED	• SR444 (ASILD)	• MCU
39.3.1	SR175	Store HV_STATUSTUS: HV_FAULT_COUNTHV_FAULT_COUNT	The BMS shall write in NV memory any update of the HV_FAULT_COUNT	TECHNICAL	A				no traced events	PROPOSED		• MCU

39.3.2	SR176	HV_STATUS Fault clearance	Once the system has entered HV_STATUS as fault, it shall only be cleared if a specific signal is received over CAN.	TE CH NIC AL	A				no traced events	PR OP OS ED			
39.4	SR177	Store failure count	The BMS shall store the faults in two counters: local and lifetime	TE CH NIC AL	A				no traced events	PR OP OS ED			
39.4.1	SR185	Keep track of lifetime fault counts	Lifetime counts shall be stored on non-volatile memory, and shall not be reset at any time.	TE CH NIC AL	A				no traced events	PR OP OS ED			

39.	SR18	Local fault counter	Local faults shall be stored for xxx days, post which the counter shall be reset. This counter shall keep track of the number of faults occurred in the past xxx days. The BMS shall clear the local fault counter if no new fault is detected within xxx days of the previous one.	TE CH NIC AL	A				no traced events	PR OP OS ED			
39.	SR18		The BMS shall clear the local fault counter if no new fault is detected within xxx seconds of the previous one.	TE CH NIC AL	A				no traced events	PR OP OS ED			
40	SR18	Permanent HV FAILURE disconnect	Open HV Switch at HV FAILURE and store in NV memory so the action is permanent	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 01 5 (ASIL B)	• MCU • FET / Contactor Driver • FET / Contactor	

40.1	SR189	Open switches at HV_STA TUS: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag HV_STATUS set FAILURE	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 449 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
40.2	SR190	Store HV_STA TUS: FAILURE	The BMS shall write in NV memory if Flag HV_STATUS set FAILURE	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 447 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
41.1	SR191	Permane nt TR FAILURE disconne ct	Open HV Switch at TR FAILURE and store in NV memory so the action is permammen t	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 015 (AS IL B) • SR 005 (AS IL B)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
41.1	SR192	Open switches at TR_STAT US: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag TR_STATUS set FAILURE	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 451 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
41.2	SR193	Store TR_STAT US: FAILURE	The BMS shall write in NV memory if Flag TR_STATUS set FAILURE	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor

42	SR19 4	TR FAULT to FAILURE timeout	Upon detection of a FAULT by the TR detection algorithm initiate a timer. Upon elapsing of pre-programmed time assign a FAILURE	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 00 5 (AS IL B)	• SR 03 1 (AS IL B)	• MCU
42. 1	SR19 5	TR_STATUS: FAULT	The BMS shall set the Flag TR_STATUS to FAULT upon a detection of the event via the TR detection algorithm. The parameters of this algorithm shall be stored in the configuration file	TE CH NIC AL	B				no traced events	PR OP OS ED			• MCU

42.2	SR196	TR_STAT US: NORMAL	The BMS shall set the Flag TR_STATUS to NORMAL upon clearing of the event if either of the conditions are met: 1. The TR detection algorithm indicates that no thermal runaway is present anymore 2. Reception of relevant signal over CAN	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
42.3	SR197	TR_FAIL URE_TI MEOUT ,	While on TR_STATUS on FAULT, the BMS shall initiate a timer of duration as specified in configuration parameter TR_FAILURE_TIMEOUT. On expiration of the counter TR_STATUS Flag shall be set to FAILURE if FAULT is still persisting	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU

43	SR19 8	Temporary disconnect the battery if fault has been detected related to temperature		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 45 2 (AS IL D) • SR 45 3 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
44	SR19 9	Temporary disconnect the battery if fault has been detected related to cell voltages		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 45 4 (AS IL D) • SR 45 5 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
45	SR20 0	Temporary disconnect the battery if fault has been detected related to battery voltage		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 45 6 (AS IL D) • SR 45 7 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor

46	SR20 1	Temporary disconnect the battery if fault has been detected related to high imbalance detected in the battery	The BMS shall set the signal(s) to _____ if the voltage imbalance (i.e. voltage difference) between cell(s) at the lowest voltage, and the cell(s) at the highest voltage exceeds xxx mV for atleast xxx ms duration.	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 45 8 (AS IL D)	• SR 45 7 (AS IL B)	• FET / Contactor Driver (ASIL B)
47	SR20 2	Temporary disconnect the battery if fault has been detected related to battery current		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 01 1 (AS IL B)	• SR 01 1 (AS IL B)	• FET / Contactor Driver (ASIL B)

47.1	SR203	Open switches at BAT CU RR STA TUS: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag BAT_CURR_STATUS set to any of the following: - OVERCURR ENT_CHAR GE - OVERCURR ENT_DISCHARGE - SHORT_CHARGE - SHORT_DISCHARGE	TE CH NIC AL	B				no traced events	PR OP OS ED				• FET / Contactor Driver (ASIL B) • MCU • FET / Contactor
47.2	SR204	Close switches at BAT CU RR STA TUS: NORMAL	The BMS shall assign signal(s) as to close the HV switches of the battery upon Flag BAT_CURR_STATUS set to NORMAL if no other protections are activated that require open HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor

48	SR205	Continuously monitor BMS internal communications	The controller shall implement mechanisms to monitor the communication status, and detect anomalies between the following: 1. Controller to AFE(s) 2. Controller to current sensor IC 3. Controller to SBC 4. Controller to HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED		• SR019 (ASIL B)	• MCU
48.1	SR206	CRC on internal communication	The AFE to AFE and AFE, BJB, SBC to MCU communication shall include CRC to detect possible communication errors	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR460 (ASIL D)	• MCU • SBC (ASIL B) • AFE • BJB IC	
48.2	SR207	EDC on internal communication	The AFE to AFE and AFE, BJB, SBC to MCU communication shall include EDC to correct possible communication errors	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU • BJB IC • SBC (ASIL B) • AFE	

48.3	SR208	Periodic external communication timers	The BMS shall keep timers associated to periodic communication packets with external controller and reset them for every packet that was successful received	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR462 (ASIL D)	• MCU
48.4	SR209	Periodic internal communication timers	The BMS shall keep timers associated to periodic internal communication packets between AFE, BJB, SBC to MCU and reset them for every packet that was successful received	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR463 (ASIL D)	• MCU
48.5	SR210	Retry communication	The BMS shall retry internal communication xxx times in case internal communication failures are encountered	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU

48.	SR21	The BMS shall raise flag COMM ERROR in case of continued failure	The BMS shall set flag COMM ERROR in case there is continued internal communication failure	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
49	SR21	Notify the driver and passengers about BMS internal communication error		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 46 6 (AS IL D)	• SR 02 9 (AS IL B)		• MCU
50	SR21	Temporary disconnect the battery if internal communication is faulty		TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 46 4 (AS IL D)	• SR 02 8 (AS IL B)	• SR 46 5 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor

50.1	SR214	Open switches at INT_CO M_STAT US: TIMEOUT T	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag INT_COM_S TATUS set to any of the following: - AFE_TIMEOUT UT - BJB_TIMEOUT UT - SBC_TIMEOUT UT	TE CH NIC AL	B				no traced events	PR OP OS ED					• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
50.2	SR215	Close switches at INT_CO M_STAT US: NORMAL	The BMS shall assign signal(s) as to close the HV switches of the charger and the battery upon a INT_COM_S TATUS to NORMAL if no other protections are activated that require open HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED					• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor

50.	SR21 3	Open switches at COM_ST ATUS: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag COM_STAT US set to any of the following: - COM_FAILURE_AFE_AF E - COM_FAILURE_AFE_MCU - COM_FAILURE_BJB_MCU - COM_FAILURE_SBC_MCU	TE CH NIC AL	B				no traced events	PR OP OS ED					• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
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50.	SR21 4	Close switches at COM_ST ATUS: WARNIN G or NORMAL	The BMS shall assign signal(s) as to close the HV switches of the battery and charger upon Flag COM_STAT US set to any of the following: - COM_WARN_AFE_AFE - COM_WARN_AFE MCU - COM_WARN_BJB MCU - COM_WARN_SBC MCU - NORMAL if no other protections are activated that require open HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
51	SR21 8	Protect against SW errors by use of adequate SW design approach		TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 01 7 (AS IL B)	• MCU	

51.1	SR219	Use of 2-level software architecture	The software architecture shall be atleast 2-level, and can be based on the EGAS architecture concept.	TECHNICAL	B				no traced events	PROPOSED				• MCU	
52.0	SR220	The BMS shall receive external commands and send external information over CAN		TECHNICAL	B				no traced events	PROPOSED	• SR467 (ASIL D)	• SR468 (ASIL D)	• SR469 (ASIL D)	• SR470 (ASIL D)	• MCU • CAN Transceiver • FET / Contactor Driver (ASIL B) • FET / Contactor
52.1	SR221	Flags over CAN	The BMS shall periodically broadcast packets with all Flags	TECHNICAL	B				no traced events	PROPOSED				• MCU • CAN Transceiver	
52.2	SR222	E2E protected CAN	The BMS shall include E2E protected CAN communication	TECHNICAL	B				no traced events	PROPOSED				• MCU	

52.3	SR22	Open HV switch	The BMS shall assign signal(s) as to open the HV switches of the charger and/or the battery upon a reception of valid command from the external controller including HV_SWITCH Flag to OPEN	TE CH NIC AL	B					no traced events	PR OP OS ED					• MCU • FET / Contactor Driver (ASIL B) • CAN Transciever • FET / Contactor
52.4	SR22	Permanent Flag	The BMS shall store in NV memory Flags upon reception of special store request packet. Storing in NV memory shall only be allowed for Flags requiring open HV switches.	TE CH NIC AL	B					no traced events	PR OP OS ED					• MCU

52.5	SR225	Close HV switch	The BMS shall assign signal(s) as to close the HV switches of the charger and/or the battery upon a reception of valid command from the external controller including HV_SWITCH Flag to Close	TECHNICAL	B				no traced events	PROPOSED				• MCU • CAN Transceiver • FET / Contactor Driver (ASIL B) • FET / Contactor
52.6	SR226	Prevent BMS failures related to production quality		TECHNICAL	B				no traced events	PROPOSED			• SR017 (ASIL B)	• Battery Management System
52.6.1	SR227	PCB manufacturing	Shall be class 2 or higher grade	TECHNICAL	B				no traced events	PROPOSED				• Battery Management System
53	SR228	The BMS shall keep track and act upon internal and external events		TECHNICAL	B				no traced events	PROPOSED			• SR017 (ASIL B)	• MCU

53.1	SR229	Flags	The BMS shall keep track of events that represent that current state of the BMS in digital representations called Flags	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
54.0	SR230	The BMS shall provide means of measurement calibration		TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 017 (AS IL B)		• MCU
54.1.1	SR231	Store calibration	The BMS shall include sufficient NV memory to store the calibration data	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
54.2.2	SR232	Retrieve configuration & Flags at boot	At boot the BMS will retrieve the calibration data from NV memory	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU
54.3.3	SR233	Program configuration & Flags	Calibration data in NV memory shall be able to be programmed by the BMS in calibration upload mode	TE CH NIC AL	B				no traced events	PR OP OS ED				• MCU • CAN Transceiver

55	SR23 8	Temporary disconnect the battery if fault has been detected related to battery short circuit	Disconnect the battery if short-circuit is detected	TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 01 1 (AS IL B)	• MCU • FET / Contactor Driver (ASIL B) • Short- circuit detection • FET / Contactor
55.1	SR23 9	Close switches upon latch signal true	The BMS shall assign signal(s) as to close the HV switches of the battery upon either of the following conditions: 1. Elapsing of timer CURRENT_INTEGRATOR_OPEN_TIME held in configuration parameter in case Current Integrator error is relieved due to previous HV switch opening action 2. Reception of _____ signal over CAN	TE CH NIC AL	B				no traced events	PR OP OS ED		• MCU • FET / Contactor Driver (ASIL B) • Short- circuit detection • FET / Contactor	

55.	SR24 2	Short-circuit definition	The BMS shall assign signal(s) as to open the HV switches of the battery upon detecting instantaneous current higher than xxx A, within xxx us.	TE CH NIC AL	B				no traced events	PR OP OS ED				• FET / Contactor Driver (ASIL B) • Short-circuit detection • FET / Contactor
56	SR24 1	Stop balancing battery	The BMS shall stop balancing the cells while the Flag CELL_BALANCE_STATUS is in state STOP_BALANCING or in cases when balancing are not being met	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 47 1 (AS IL D)	• SR 01 6 (AS IL B)	• SR 47 2 (AS IL D)	• MCU • AFE • TPL Transceiver

57	SR24 2	Current integrator	The BMS shall be equipped with current integrator with SW selectable integration period of a range of xxx to xxx ms. In case the integration period is SW selectable the BMS shall select the value stored in configuration parameter.	TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 01 2 (ASIL B)	• MCU • Short-circuit detection
58	SR24 3	SW HV switch timing	Upon actuation signal provided, the HV switches shall not take more than xxx ms and xxx ms to open and close respectively .	TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 02 2 (ASIL B)	• FET / Contactor Driver (ASIL B) • MCU • FET / Contactor
59	SR24 4	AIS-156 and AIS_004 compliance		TE CH NIC AL	N O N E				no traced events	PR OP OS ED			• Battery Management System
60	SR24 5	Provide protections for internal voltage faults	Provide protections for cases where isolation failure can occur (optocouplers, isolated transcievers, etc.)	TE CH NIC AL	B				no traced events	PR OP OS ED		• SR 02 6 (ASIL B)	• Battery Management System

61	SR24 6	Set status to Unbalanced	The BMS shall set the CELL_BALANCE_STATUS to UNBALANCE_D if the cell voltage difference between the cell(s) with minimum voltage and those with maximum voltage exceeds xxx mV.	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 47 4 (AS IL D)	• SR 01 6 (AS IL B)
62	SR24 7	The system shall use suitable sensors to detect thermal runaway		TE CH NIC AL	D				no traced events	PR OP OS ED	• SR 00 5 (AS IL B)	
63	SR25 2	Open switches at HV_SWITCH_STATUS: FAILURE	The BMS shall assign signal(s) as to open the HV switches of the battery upon Flag HV_SWITCH_STATUS set to FAILURE	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 47 7 (AS IL D) • SR 47 8 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor

64	SR25 3	Close switches at HV_SWITC TCH_ST ATUS: NORMAL	The BMS shall assign signal(s) as to close the HV switches of the battery upon Flag HV_SWITC H_STATUS set to NORMAL if no other protections are activated that require open HV switches	TE CH NIC AL	B				no traced events	PR OP OS ED	• SR 47 9 (AS IL D) • SR 48 0 (AS IL D)	• MCU • FET / Contactor Driver (ASIL B) • FET / Contactor
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65	SR312	[A] Continuously monitor battery voltage	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 25 1 (AS IL B) • SR 26 0 (AS IL B) • SR 25 7 (AS IL B) • SR 10 4 (AS IL B) • SR 26 9 (AS IL B) • SR 28 2 (AS IL B) • SR 54 8 (AS IL B) • SR 56 1 (AS IL B) •
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28-Mar-2025 12:08 pm

												SR 55 9 (AS IL B)
65. 1	SR30 7	[A] Battery Voltage Monito ring Perform ance		TE CH NIC AL	D			no traced events	PR OP OS ED	• G0 02 (AS IL B)		
65. 1.1	SR30 8	[A] Battery Voltage Range	The BMS shall measure battery voltage with range at least of 0 to xxxV.	TE CH NIC AL	D			no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 66 3 (AS IL D) • SR 66 4 (AS IL D)	

65.	SR30	[A] Battery Voltage Accuracy	The BMS shall measure battery voltage with accuracy of xxx mV, across operating temperature -25 degree celcius to 125 degree celcius	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 65 9 (AS IL D) • SR 66 0 (AS IL D) • SR 66 1 (AS IL D) • SR 66 2 (AS IL D) • SR 66 5 (AS IL D)		
65.	SR31	[A] Battery Voltage Resolution	The BMS shall measure battery voltage with at most and resolution of xxxmV.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 65 8 (AS IL D)		

65.	SR31	[A]	Battery Voltage Samplin g	The BMS shall measure battery voltage at a sampling rate of at least xxx sample/sec.	TE CH NIC AL	D					no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 65 6 (Q M) • SR 65 7 (AS IL D)		
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66	SR318	[A] Continuously monitor battery temperature		TE CH NIC AL	D				no traced events	PR OP OS ED	• G02 (AS IL B)		• SR 035 (AS IL B) • SR 104 (AS IL B) • SR 051 (AS IL B) • SR 038 (AS IL B) • SR 269 (AS IL B) • SR 282 (AS IL B) • SR 330 (AS IL B) • SR 561 (AS IL B) •
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28-Mar-2025 12:08 pm

												SR 55 9 (AS IL B)
66.1	SR31 3	[A] Battery Tempera ture Monitor		TE CH NIC AL	D			no traced events	PR OP OS ED	• G0 02 (AS IL B)		
66.1.1	SR31 4	[A] Battery Tempera ture Range	The BMS shall measure battery Temperatur e with range at least of 0 to xxxV.	TE CH NIC AL	D			no traced events	PR OP OS ED	• G0 02 (AS IL B)		
66.1.2	SR31 5	[A] Battery Tempera ture Accuracy	The BMS shall measure battery Temperatur e with accuracy of xxx mV.	TE CH NIC AL	D			no traced events	PR OP OS ED	• G0 02 (AS IL B)		
66.1.3	SR31 6	[A] Battery Tempera ture Resoluti on	The BMS shall measure battery Temperatur e with at most and resolution of xxx °C	TE CH NIC AL	D			no traced events	PR OP OS ED	• G0 02 (AS IL B)		
66.1.4	SR31 7	[A] Battery Tempera ture Samplin g	The BMS shall measure battery Temperatur e vat a sampling rate of at least xxx sample/sec.	TE CH NIC AL	D			no traced events	PR OP OS ED	• G0 02 (AS IL B)		

67	SR324	[A] Continuously monitor battery current.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G02 (AS IL B)		• SR 274 (AS IL B) • SR 104 (AS IL B) • SR 277 (AS IL B) • SR 269 (AS IL B) • SR 282 (AS IL B) • SR 276 (AS IL B) • SR 559 (AS IL B) • SR 561 (AS IL B) •
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28-Mar-2025 12:08 pm

													SR 56 0 (AS IL D) • SR 58 3 (AS IL D) • SR 59 7 (AS IL B) • SR 59 9 (AS IL B)
67.1	9	[A] Battery Current Monitor		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		
67.1.1	0	[A] Battery Current Range	The BMS shall measure battery Current with range at least of 0 to xxxV.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		
67.1.2	1	[A] Battery Current Accuracy	The BMS shall measure battery Current with accuracy of xxx mV.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		

67. 1.3	SR32 2	[A] Battery Current Resoluti on	The BMS shall measure battery Current with at most and resolution of xxxmV.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)			
67. 1.4	SR32 3	[A] Battery Current Samplin g	The BMS shall measure battery Current at a sampling rate of at least xxx sample/sec.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 66 6 (AS IL D)	• SR 66 8 (AS IL D)	• SR 66 9 (AS IL D)
68	SR32 5	Sned data over UART		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 28 4 (AS IL B)	
69	SR32 6	Sned data over CAN		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 28 4 (AS IL B)	
70	SR32 9	[F] Send data over CAN to IPC		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 28 3 (AS IL B)	

71	SR334	[F] Send data over CAN within xxx msec after detection of temperature fault.		TECHNICAL	D				no traced events	PROPOSED	• G002 (ASIL B)		• SR123 (ASIL B)
72	SR335	Sned data over CAN		TECHNICAL	D				no traced events	PROPOSED	• G002 (ASIL B)		• SR271 (ASIL B)
73	SR336	Sned data over CAN		TECHNICAL	D				no traced events	PROPOSED	• G002 (ASIL B)		• SR248 (ASIL B)
74	SR445	Sned data over UART		TECHNICAL	D				no traced events	PROPOSED	• G002 (ASIL B)		• SR271 (ASIL B)
75	SR446	Sned data over UART		TECHNICAL	D				no traced events	PROPOSED	• G002 (ASIL B)		• SR248 (ASIL B)
76	SR537	[E] BMS shall send max permissible charging and dicharging current limits every xxx sec.		TECHNICAL	D				no traced events	PROPOSED	• G002 (ASIL B)		• SR104 (ASIL B) • SR035 (ASIL B)

28-Mar-2025 12:08 pm

77	SR538	[E] BMS shall send max permissible charging and discharging current limits every xxx sec.	TECHNICAL	D				no traced events	PROPOSED	• G002 (ASIL B)		• SR266 (ASIL D)
78	SR539	[E] BMS shall send max permissible charging and discharging current limits every xxx sec.	TECHNICAL	D				no traced events	PROPOSED	• G002 (ASIL B)		• SR279 (ASIL D)
79	SR542	[D] FHTI should be less than xxx sec[FTTI]	TECHNICAL	D				no traced events	PROPOSED			

80	SR549	[B] The rate of change of voltage must not be more than xxx mV/msec for more than yyy sec		TE CH NIC AL	D				no traced events	PR OP OS ED	• G002 (AS IL B)		• SR548 (AS IL B)
81	SR551	[B] The rate of change of voltage must not be more than xxx.		TE CH NIC AL	D				no traced events	PR OP OS ED	• G002 (AS IL B)		• SR330 (AS IL B)
82	SR565	[C] Permanently disconnect the battery within xx msec of receiving the signal.		TE CH NIC AL	D				no traced events	PR OP OS ED	• G002 (AS IL B)		• SR556 (AS IL B) • SR560 (AS IL D) • SR552 (AS IL B)

83	SR567	[F] Send data over CAN within xxx msec after detection of thermal runaway .		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 564 (AS IL B)
84	SR568	[G] Send data over CAN		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 555 (AS IL B)
85	SR569	[G] Send data over UART		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 555 (AS IL B)
86	SR570	[A] Continuously monitor cell voltage		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 571 (AS IL D)	• SR 251 (AS IL B)
87	SR571	[A] Cell Voltage Monitoring Performance		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 570 (AS IL D)
87.1	SR572	[A] Cell Voltage Range	The BMS shall measure battery voltage with range at least of 0 to xxxV.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		

87.2	SR573	[A] Cell Voltage Accuracy	The BMS shall measure battery voltage with accuracy of xxx mV, across operating temperature -25 degree celcius to 125 degree celcius	TE CH NIC AL	D				no traced events	PR OP OS ED	• G002 (AS ILB)		
87.3	SR574	[A] Cell Voltage Resolution	The BMS shall measure battery voltage with at most and resolution of xxxmV.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G002 (AS ILB)		
87.4	SR575	[A] Cell Voltage Sampling	The BMS shall measure cell voltage at a sampling rate of at least xxx sample/sec.	TE CH NIC AL	D				no traced events	AS SU ME D	• G002 (AS ILB)		
88	SR576			TE CH NIC AL	D				no traced events	PR OP OS ED			

89	SR57 7	The BMS shall transition from the safe state to the operational state when the battery voltage remains below the overvoltage threshold of [XXX] V for a duration of [XXX] time, ensuring fault recovery conditions are met.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 26 8 (AS IL B)
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90	SR57 8	he BMS shall transition from the safe state to the operational state when the battery voltage remains above the undervoltage threshold of [XXX] V for a duration of [XXX] time, ensuring fault recovery conditions are met	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 26 7 (AS IL B)
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91	SR579	The BMS shall transition from the safe state to the operational state when the battery temperature remains above the undetermined temperature threshold of [XXX]°C for a duration of [XXX] time, ensuring fault recovery conditions are met.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G002 (ASIL B)		• SR073 (ASIL B)
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92	SR580	The BMS shall transition from the safe state to the operational state when the battery temperature remains below the overtemperature threshold of [XXX]°C for a duration of [XXX] time, ensuring fault recovery conditions are met.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G002 (ASIL B)		• SR102 (ASIL B)
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93	SR58 1	The BMS shall transition from the safe state to the operational state when the charging current remains below the overcurrent threshold of [XXX] A for a duration of [XXX] time, ensuring fault recovery conditions are met.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 28 1 (AS IL B)
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94	SR58 2	The BMS shall transition from the safe state to the operational state when the discharging current remains below the overcurrent threshold of [XXX] A for a duration of [XXX] time, ensuring fault recovery conditions are met.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 28 0 (AS IL B)
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95	SR584	[G] The BMS shall give warning to driver regarding the increasing temperature so that the driver and can take precautionary actions and avoid the fault occurrence.	TE CH NIC AL	D					no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 61 6 (AS IL D)	• SR 24 8 (AS IL B)	• SR 61 7 (AS IL D)	• SR 03 5 (AS IL B)
96	SR585	[G] The BMS shall give warning to driver regarding the increasing voltage so that the driver and can take precautionary actions and avoid the fault occurrence.	TE CH NIC AL	D					no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 61 2 (AS IL D)	• SR 27 1 (AS IL B)	• SR 61 3 (AS IL D)	• SR 25 1 (AS IL B)

97	SR586	[G] The BMS shall give warning to driver regarding the breach in current SOA so that the driver and can take precautionary actions and avoid the fault occurrence.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 61 8 (AS IL B)	• SR 28 4 (AS IL B)	• SR 27 4 (AS IL B)
98	SR588	[C] The BMS shall transit to safe state within xxx msec after detecting under voltage fault signal.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 26 7 (AS IL B)	• SR 27 2 (AS IL B)	• SR 27 2 (AS IL B)
99	SR589	[C] The BMS shall transit to safe state within xxx msec after detecting over voltage fault signal.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 26 8 (AS IL B)	• SR 27 2 (AS IL B)	• SR 27 2 (AS IL B)

10 0	SR59 0	[C] The BMS shall transit to safe state within xxx msec after receiving under temperature fault signal.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 07 3 (AS IL B) • SR 24 9 (AS IL B)
10 1	SR59 1	[C] The BMS shall transit to safe state within xxx msec after receiving the over-current fault signal during discharging.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 28 1 (AS IL B) • SR 28 5 (AS IL B)
10 2	SR59 2	[C] The BMS shall transit to safe state within xxx msec after receiving the over-current fault signal during charging.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 28 0 (AS IL B) • SR 28 5 (AS IL B)

10 3	SR59 3	[C] The BMS shall transit to safe state within xxx msec after receiving the short circuit fault signal.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 59 4 (AS IL D) • SR 60 3 (AS IL B) • SR 60 0 (AS IL B)
10 4	SR59 5	Temporary disconnect recovery for SC	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 59 4 (AS IL D)
10 5	SR32 8	[F] Send data over CAN within xxx msec after detection of current fault.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 28 3 (AS IL B)
10 6	SR59 6	SM: Recovery out of permanent failure shall only be possible through service station intervention.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 55 6 (AS IL B)

10 7	SR54 4	[B] The BMS shall detect under-voltage fault within xxx msec of occurrence.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 26 0 (AS IL B) • SR 27 2 (AS IL B) • SR 26 7 (AS IL B) • SR 27 0 (AS IL B)
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10 8	SR58 7	[B] The BMS shall detect short circuit fault within xxx usec of occurrence.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 58 3 (AS IL D) • SR 59 9 (AS IL B) • SR 60 0 (AS IL B) • SR 60 3 (AS IL B) • SR 60 2 (AS IL B)
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10 9	SR56 6	[B] The BMS shall detect possibility of thermal runaway within xx msec of occurrence of such conditions	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 56 1 (AS IL B) • SR 55 6 (AS IL B) • SR 55 2 (AS IL B) • SR 56 4 (AS IL B)	
11 0	SR60 4	[G] The BMS shall give warning to driver regarding the increasing temperature so that the driver and can take precautionary actions and avoid the fault occurrence.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 55 5 (AS IL B) • SR 55 9 (AS IL B)	

11 1	SR60 5	[G] The BMS shall give warning to driver regarding the increasing current so that the driver can take precautionary actions and avoid the fault occurrence.	TE CH NIC AL	D				no traced events	PR OP OS ED				
11 2	SR60 6	[F] Send data over CAN within xxx msec after detection of sshort circuit.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 60 2 (AS IL B)	

11 3	SR60 7	[G] The BMS shall give warning to driver regarding the increasing temperature so that the driver and can take precautionary actions and avoid the fault occurrence.	TE CH NIC AL	D					no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 61 4 (AS IL D)	• SR 24 8 (AS IL B)	• SR 61 03 5 (AS IL D)
11 4	SR60 8	[G] The BMS shall give warning to driver regarding the increasing voltage so that the driver and can take precautionary actions and avoid the fault occurrence.	TE CH NIC AL	D					no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 61 0 (AS IL D)	• SR 27 1 (AS IL B)	• SR 61 25 1 (AS IL D)

11 5	SR60 9	[G] The BMS shall give warning to driver regarding the breach in current SOA so that the driver and can take precautionary actions and avoid the fault occurrence.	TE CH NIC AL	D					no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 62 1 (AS IL D)	SR 27 4 (AS IL B)	SR 27 4 (AS IL B)
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11 6	SR61 0	The BMS shall trigger a warning to the driver when the battery voltage drops below the undervoltage warning threshold of [XXX] V for a duration of [XXX] time, allowing precautionary actions to be taken."	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 60 8 (AS IL D)
11 7	SR61 1	The BMS shall clear the undervoltage warning when the battery voltage rises above [XXX] V and remains stable for [XXX] time.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 60 8 (AS IL D)

11 8	SR61 2	The BMS shall trigger a warning to the driver when the battery voltage exceeds the overvoltage warning threshold of [XXX] V for a duration of [XXX] time, allowing precautionary actions to be taken.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 58 5 (AS IL D)
11 9	SR61 3	The BMS shall clear the overvoltage warning when the battery voltage returns below [XXX] V and remains stable for [XXX] time.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 58 5 (AS IL D)

12 0	SR61 4	The BMS shall trigger a warning to the driver when the battery temperature drops below the undetermined temperature warning threshold of [XXX]°C for a duration of [XXX] time, allowing precautionary actions to be taken.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 60 7 (AS IL D)
12 1	SR61 5	The BMS shall clear the undetermined temperature warning when the battery temperature rises above [XXX]°C and remains stable for [XXX] time.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 60 7 (AS IL D)

28-Mar-2025 12:08 pm

12	SR61 6	The BMS shall trigger a warning to the driver when the battery temperature exceeds the overtemperature warning threshold of [XXX]°C for a duration of [XXX] time, allowing precautionary actions to be taken.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 58 4 (AS IL D)
12 3	SR61 7	The BMS shall clear the overtemperature warning when the battery temperature falls below [XXX]°C and remains stable for [XXX] time.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 58 4 (AS IL D)

12 4	SR61 8	The BMS shall clear the charging overcurrent warning when the charging current remains below [XXX] A and stable for [XXX] time.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 58 6 (AS IL D)
12 5	SR61 9	The BMS shall trigger a warning to the driver when the charging current exceeds the overcurrent warning threshold of [XXX] A for a duration of [XXX] time, allowing precautionary actions to be taken.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 58 6 (AS IL D)

12 6	SR62 0	The BMS shall trigger a warning to the driver when the discharging current exceeds the overcurrent warning threshold of [XXX] A for a duration of [XXX] time, allowing precautionary actions to be taken.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 60 9 (AS IL D)
12 7	SR62 1	The BMS shall clear the discharging overcurrent warning when the discharging current remains below [XXX] A and stable for [XXX] time.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 60 9 (AS IL D)

12 8	SR62 2	SM: Recover y out of permanent failure shall only be possible through service station intervention.		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 60 3 (AS IL B)
12 9	SR54 5	[B] The BMS shall detect over-voltage fault within xxx msec of occurrence.		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 25 7 (AS IL B) • SR 27 2 (AS IL B) • SR 26 8 (AS IL B) • SR 27 0 (AS IL B)	• SR 25 7 (AS IL B) • SR 27 2 (AS IL B) • SR 26 8 (AS IL B) • SR 27 0 (AS IL B)
13 0	SR33 1	[F] Send data over CAN to IPC		TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 27 0 (AS IL B)	• SR 27 0 (AS IL B)

13 1	SR33 3	[F] Send data over CAN within xxx msec after detection of voltage fault.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 27 0 (AS IL B)
13 2	SR33 2	[F] Send data over CAN to IPC	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 12 3 (AS IL B)
13 3	SR54 3	[B] The BMS shall detect over-temperature fault within xxx msec of occurrence.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 03 8 (AS IL B) • SR 24 9 (AS IL B) • SR 12 3 (AS IL B) • SR 10 2 (AS IL B)	• SR 03 8 (AS IL B) • SR 24 9 (AS IL B) • SR 12 3 (AS IL B) • SR 10 2 (AS IL B)

13 4	SR54 0	[B] The BMS shall detect under-temperature fault within xxx msec of occurrence.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 05 1 (AS IL B) • SR 24 9 (AS IL B) • SR 12 3 (AS IL B) • SR 07 3 (AS IL B)
13 5	SR54 1	[C] The BMS shall transit to safe state within xxx msec after receiving over temperature fault signal.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 10 2 (AS IL B) • SR 24 9 (AS IL B)

13 6	SR54 7	[B] The BMS shall detect over-current fault within xxx msec of occurrence during charging.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 27 7 (AS IL B) • SR 28 3 (AS IL B) • SR 28 5 (AS IL B) • SR 28 0 (AS IL B)
13 7	SR54 6	[B] The BMS shall detect over-current fault within xxx msec of occurrence during discharging.	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)		• SR 27 6 (AS IL B) • SR 28 3 (AS IL B) • SR 28 5 (AS IL B) • SR 28 1 (AS IL B)

13 8	SR62 3	SM: Bms shall implement method to detect and react to short circuit fault through hardware without requiring intervention of software .	TE CH NIC AL	D				no traced events	PR OP OS ED	• G0 02 (AS IL B)	• SR 59 9 (AS IL B)
13 9	SR62 4	In case of existance of any permanent failure, the system shall not recover	TE CH NIC AL	D				no traced events	PR OP OS ED		
14 0	SR62 5	The BMS shall implement the following states: "NORMAL", "SLEEP", "DEEPSLEEP", "WARNING", "FAULT". "FAULT_PERMANENT", "LIMP"	TE CH NIC AL	D				no traced events	PR OP OS ED	• SR 62 6 (AS IL D)	

14 1	SR62 6	<TRANS ITION between states>		TE CH NIC AL	D				no traced events	PR OP OS ED			• SR 62 5 (AS IL D)
14 2	SR62 7	SM: Inline controlla ble fuse / switch in series with mosfets	From FMEA: mosfets short	TE CH NIC AL	D				no traced events	PR OP OS ED			
14 3	SR62 8	SM: Mosfet control feedback mechani sm		TE CH NIC AL	D				no traced events	PR OP OS ED			
14 4	SR62 9	SM: Precharg e control feedback mechani sm		TE CH NIC AL	D				no traced events	PR OP OS ED			
14 5	SR63 0	SM: measure voltage of different voltage rails		TE CH NIC AL	D				no traced events	PR OP OS ED			
14 6	SR63 1	SM: emergen cy operatio n FHTI definitio n	Software level 2 reaction time interval	TE CH NIC AL	D				no traced events	PR OP OS ED			
14 7	SR63 2	Reliabilit y requirem ent: precharg e resistor	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			

14 8	SR63 3	Reliability requirement: precharge mosfet	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
14 9	SR63 4	Reliability requirement: fuse	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
15 0	SR63 5	Reliability requirement: main mosfets	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
15 1	SR63 6	Reliability requirement: signal connectors	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
15 2	SR63 7	Reliability requirement shunt	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
15 3	SR63 8	Reliability requirement power connector	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
15 4	SR63 9	Access control		TE CH NIC AL	D				no traced events	PR OP OS ED			
15 5	SR64 0	cyber security		TE CH NIC AL	D				no traced events	PR OP OS ED			
15 6	SR64 1	Boot Loader		TE CH NIC AL	D				no traced events	PR OP OS ED			
15 7	SR64 2	Size		TE CH NIC AL	D				no traced events	PR OP OS ED			
15 8	SR64 3	Size		TE CH NIC AL	D				no traced events	PR OP OS ED			

28-Mar-2025 12:08 pm

15 9	SR64 4	Boot Loader		TE CH NIC AL	D				no traced events	PR OP OS ED			
16 0	SR64 5	Reliabilit y requirem ent: precharg e mosfet	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
16 1	SR64 6	cyber security		TE CH NIC AL	D				no traced events	PR OP OS ED			
16 2	SR64 7	Reliabilit y requirem ent power connecto r	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
16 3	SR64 8	Access control		TE CH NIC AL	D				no traced events	PR OP OS ED			
16 4	SR64 9	Reliabilit y requirem ent: signal connecto rs	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
16 5	SR65 0	Reliabilit y requirem ent: precharg e resistor	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
16 6	SR65 1	Reliabilit y requirem ent:fuse	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
16 7	SR65 2	Reliabilit y requirem ent: main mosfets	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			
16 8	SR65 3	Reliabilit y requirem ent shunt	<move to BMS TSR>	TE CH NIC AL	D				no traced events	PR OP OS ED			